DDR2 Unbuffered SDRAM MODULE

240pin Unbuffered Module based on 2Gb A-die

64/72-bit Non-ECC/ECC

68FBGA with Lead-Free and Halogen-Free

(RoHS compliant)

Table of Contents

1.0 DDR2 Unbuffered DIMM Ordering Information 4
2.0 Features 4
3.0 Address Configuration 4
4.0 x64 DIMM Pin Configurations (Front side/Back side) 5
5.0 x72 DIMM Pin Configurations (Front side/Back side) 6
6.0 Pin Description 6
7.0 Input/Output Function Description 7
8.0 Functional Block Diagram : 8
8.1 4GB, 512Mx64 Module - M378T5263AZ(H)3 8
8.2 4GB, 512Mx72 ECC Module - M391T5263AZ(H)3 9
9.0 Absolute Maximum DC Ratings 10
10.0 AC & DC Operating Conditions 10
10.1 Recommended DC Operating Conditions (SSTL - 1.8) 10
10.2 Operating Temperature Condition 11
10.3 Input DC Logic Level 11
10.4 Input AC Logic Level 11
10.5 AC Input Test Conditions 11
11.0 IDD Specification Parameters Definition 12
12.0 Operating Current Table : 13
12.1 M378T5263AZ(H)3 : 4GB(256Mx8 *16) Module 13
12.2 M391T5263AZ(H)3 : 4GB(256Mx8 *18) ECC Module 13
13.0 Input/Output Capacitance 14
14.0 Electrical Characteristics & AC Timing for DDR2-800/667/533 14
14.1 Refresh Parameters by Device Density 14
14.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin 14
14.3 Timing parameters by speed grade (DDR2-800 and DDR2-667) 15
14.4 Timing parameters by speed grade (DDR2-533) 17
15.0 Physical Dimensions : 19

Revision History

Revision	Month	Year	History
1.0	December	2007	- Initial Release
1.1	July	2008	- Applied JEDEC update(JESD79-2E) on AC timing table

1.0 DDR2 Unbuffered DIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Height
x64 Non ECC					
M378T5263AZ(H)3-CE7/F7/E6/D5	4GB	512Mx64	256Mx8(K4T2G084QA)*16	2	30mm
x72 ECC					
M391T5263AZ(H)3-CE7/F7/E6/D5	4GB	512Mx72	256Mx8(K4T2G084QA)*18	2	30mm

Note :
1. “Z” of Part number(12th digit) stands for Lead-Free products.
2. “H” of Part number(12th digit) stands for Lead-Free, Halogen-Free, and RoHS compliant products.
3. “3” of Part number(13th digit) stands for Dummy Pad PCB products.

2.0 Features

- Performance range

	E7 (DDR2-800)	F7 (DDR2-800)	E6 (DDR2-667)	D5 (DDR2-533)	Unit
Speed@CL3	400	-	400	400	Mbps
Speed@CL4	533	533	533	533	Mbps
Speed@CL5	800	667	667	533	Mbps
Speed@CL6	-	800	-	-	Mbps
CL-tRCD-tRP	5-5-5	6-6-6	5-5-5	4-4-4	CK

- JEDEC standard V_{DD} = 1.8V ± 0.1V Power Supply
- V_{DDQ} = 1.8V ± 0.1V
- 267MHz f_{CK} for 533Mb/sec/pin, 333MHz f_{CK} for 667Mb/sec/pin, 400MHz f_{CK} for 800Mb/sec/pin
- 8 Banks
- Posted $\overline{CAS}$
- Programmable $\overline{CAS}$ Latency: 3, 4, 5, 6
- Programmable Additive Latency: 0, 1 , 2 , 3, 4, 5
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/Nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination with selectable values(50/75/150 ohms or disable)
- Average Refresh Period 7.8us at lower than a T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95 °C
  - Support High Temperature Self-Refresh rate enable feature
- Package: 68ball FBGA - 128Mx8
- All of base components are Lead-Free, Halogen-Free, and RoHS compliant

Note: For detailed DDR2 SDRAM operation, please refer to Samsung’s Device operation & Timing diagram.

3.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
256Mx8(2Gb) based Module	A0-A14	A0-A9	BA0-BA2	A10

4.0 x64 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	121	V_{SS}	31	DQ19	151	V_{SS}	61	A4	181	V_{DDQ}	91	V_{SS}	211	DM5
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQ28	62	V_{DDQ}	182	A3	92	$\overline{DQS}5$	212	NC
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V_{SS}
4	DQ1	124	V_{SS}	34	DQ25	154	V_{SS}	64	V_{DD}	184	V_{DD}	94	V_{SS}	214	DQ46
5	V_{SS}	125	DM0	35	V_{SS}	155	DM3	KEY				95	DQ42	215	DQ47
6	$\overline{DQS}0$	126	NC	36	$\overline{DQS}3$	156	NC	65	V_{SS}	185	CK0	96	DQ43	216	V_{SS}
7	DQS0	127	V_{SS}	37	DQS3	157	V_{SS}	66	V_{SS}	186	$\overline{CK}0$	97	V_{SS}	217	DQ52
8	V_{SS}	128	DQ6	38	V_{SS}	158	DQ30	67	V_{DD}	187	V_{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC	188	A0	99	DQ49	219	V_{SS}
10	DQ3	130	V_{SS}	40	DQ27	160	V_{SS}	69	V_{DD}	189	V_{DD}	100	V_{SS}	220	CK2
11	V_{SS}	131	DQ12	41	V_{SS}	161	NC	70	A10/AP	190	BA1	101	SA2	221	$\overline{CK}2$
12	DQ8	132	DQ13	42	NC	162	NC	71	BA0	191	V_{DDQ}	102	NC, TEST[1]	222	V_{SS}
13	DQ9	133	V_{SS}	43	NC	163	V_{SS}	72	V_{DDQ}	192	$\overline{RAS}$	103	V_{SS}	223	DM6
14	V_{SS}	134	DM1	44	V_{SS}	164	NC	73	$\overline{WE}$	193	$\overline{S}0$	104	$\overline{DQS}6$	224	NC
15	$\overline{DQS}1$	135	NC	45	NC	165	NC	74	$\overline{CAS}$	194	V_{DDQ}	105	DQS6	225	V_{SS}
16	DQS1	136	V_{SS}	46	NC	166	V_{SS}	75	V_{DDQ}	195	ODT0	106	V_{SS}	226	DQ54
17	V_{SS}	137	CK1	47	V_{SS}	167	NC	76	$\overline{S}1$	196	A13	107	DQ50	227	DQ55
18	NC	138	$\overline{CK}1$	48	NC	168	NC	77	ODT1	197	V_{DD}	108	DQ51	228	V_{SS}
19	NC	139	V_{SS}	49	NC	169	V_{SS}	78	V_{DDQ}	198	V_{SS}	109	V_{SS}	229	DQ60
20	V_{SS}	140	DQ14	50	V_{SS}	170	V_{DDQ}	79	V_{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V_{DDQ}	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	V_{SS}
22	DQ11	142	V_{SS}	52	CKE0	172	V_{DD}	81	DQ33	201	V_{SS}	112	V_{SS}	232	DM7
23	V_{SS}	143	DQ20	53	V_{DD}	173	NC	82	V_{SS}	202	DM4	113	$\overline{DQS}7$	233	NC
24	DQ16	144	DQ21	54	NC	174	A14	83	$\overline{DQS}4$	203	NC	114	DQS7	234	V_{SS}
25	DQ17	145	V_{SS}	55	NC	175	V_{DDQ}	84	DQS4	204	V_{SS}	115	V_{SS}	235	DQ62
26	V_{SS}	146	DM2	56	V_{DDQ}	176	A12	85	V_{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{DQS}2$	147	NC	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V_{SS}
28	DQS2	148	V_{SS}	58	A7	178	V_{DD}	87	DQ35	207	V_{SS}	118	V_{SS}	238	V_{DDSPD}
29	V_{SS}	149	DQ22	59	V_{DD}	179	A8	88	V_{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V_{SS}				

NC = No Connect, RFU = Reserved for Future Use

1. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

5.0 x72 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	121	V_{SS}	31	DQ19	151	V_{SS}	61	A4	181	V_{DDQ}	91	V_{SS}	211	DM5
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQ28	62	V_{DDQ}	182	A3	92	$\overline{DQS5}$	212	NC
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V_{SS}
4	DQ1	124	V_{SS}	34	DQ25	154	V_{SS}	64	V_{DD}	184	V_{DD}	94	V_{SS}	214	DQ46
5	V_{SS}	125	DM0	35	V_{SS}	155	DM3	KEY				95	DQ42	215	DQ47
6	$\overline{DQS0}$	126	NC	36	$\overline{DQS3}$	156	NC	65	V_{SS}	185	CK0	96	DQ43	216	V_{SS}
7	DQS0	127	V_{SS}	37	DQS3	157	V_{SS}	66	V_{SS}	186	$\overline{CK0}$	97	V_{SS}	217	DQ52
8	V_{SS}	128	DQ6	38	V_{SS}	158	DQ30	67	V_{DD}	187	V_{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC	188	A0	99	DQ49	219	V_{SS}
10	DQ3	130	V_{SS}	40	DQ27	160	V_{SS}	69	V_{DD}	189	V_{DD}	100	V_{SS}	220	CK2
11	V_{SS}	131	DQ12	41	V_{SS}	161	CB4	70	A10/AP	190	BA1	101	SA2	221	$\overline{CK2}$
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	V_{DDQ}	102	NC, TEST[1]	222	V_{SS}
13	DQ9	133	V_{SS}	43	CB1	163	V_{SS}	72	V_{DDQ}	192	$\overline{RAS}$	103	V_{SS}	223	DM6
14	V_{SS}	134	DM1	44	V_{SS}	164	DM8	73	$\overline{WE}$	193	$\overline{S0}$	104	$\overline{DQS6}$	224	NC
15	$\overline{DQS1}$	135	NC	45	$\overline{DQS8}$	165	NC	74	$\overline{CAS}$	194	V_{DDQ}	105	DQS6	225	V_{SS}
16	DQS1	136	V_{SS}	46	DQS8	166	V_{SS}	75	V_{DDQ}	195	ODT0	106	V_{SS}	226	DQ54
17	V_{SS}	137	CK1	47	V_{SS}	167	CB6	76	$\overline{S1}$	196	A13	107	DQ50	227	DQ55
18	NC	138	$\overline{CK1}$	48	CB2	168	CB7	77	ODT1	197	V_{DD}	108	DQ51	228	V_{SS}
19	NC	139	V_{SS}	49	CB3	169	V_{SS}	78	V_{DDQ}	198	V_{SS}	109	V_{SS}	229	DQ60
20	V_{SS}	140	DQ14	50	V_{SS}	170	V_{DDQ}	79	V_{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V_{DDQ}	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	V_{SS}
22	DQ11	142	V_{SS}	52	CKE0	172	V_{DD}	81	DQ33	201	V_{SS}	112	V_{SS}	232	DM7
23	V_{SS}	143	DQ20	53	V_{DD}	173	NC	82	V_{SS}	202	DM4	113	$\overline{DQS7}$	233	NC
24	DQ16	144	DQ21	54	NC	174	A14	83	$\overline{DQS4}$	203	NC	114	DQS7	234	V_{SS}
25	DQ17	145	V_{SS}	55	NC	175	V_{DDQ}	84	DQS4	204	V_{SS}	115	V_{SS}	235	DQ62
26	V_{SS}	146	DM2	56	V_{DDQ}	176	A12	85	V_{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{DQS2}$	147	NC	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V_{SS}
28	DQS2	148	V_{SS}	58	A7	178	V_{DD}	87	DQ35	207	V_{SS}	118	V_{SS}	238	V_{DDSPD}
29	V_{SS}	149	DQ22	59	V_{DD}	179	A8	88	V_{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V_{SS}				

NC = No Connect, RFU = Reserved for Future Use

1. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

6.0 Pin Description

Pin Name	Description	Pin Name	Description
A0-A14	DDR2 SDRAM address bus	CK0, CK1, CK2	DDR2 SDRAM clocks (positive line of differential pair)
BA0-BA2	DDR2 SDRAM bank select	$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	DDR2 SDRAM clocks (negative line of differential pair)
RAS	DDR2 SDRAM row address strobe	SCL	I^2C serial bus clock for EEPROM
CAS	DDR2 SDRAM column address strobe	SDA	I^2C serial bus data line for EEPROM
WE	DDR2 SDRAM wirte enable	SA0-SA2	I^2C serial address select for EEPROM
$\overline{S0}$, $\overline{S1}$	DIMM Rank Select Lines	V_{DD}*	DDR2 SDRAM core power supply
CKE0,CKE1	DDR2 SDRAM clock enable lines	V_{DDQ}*	DDR2 SDRAM I/O Driver power supply
ODT0, ODT1	On-die termination control lines	V_{REF}	DDR2 SDRAM I/O reference supply
DQ0 - DQ63	DIMM memory data bus	V_{SS}	Power supply return (ground)
CB0 - CB7	DIMM ECC check bits	V_{DDSPD}	Serial EEPROM positive power supply
DQS0 - DQS8	DDR2 SDRAM data strobes	NC	Spare Pins(no connect)
DM(0-8)	DDR2 SDRAM data masks	RESET	Not used on UDIMM
$\overline{DQS0}$-$\overline{DQS8}$	DDR2 SDRAM differential data strobes	TEST	Used by memory bus analysis tools (unused on memory DIMMs)

*The V_{DD} and V_{DDQ} pins are tied to the single power-plane on PCB.

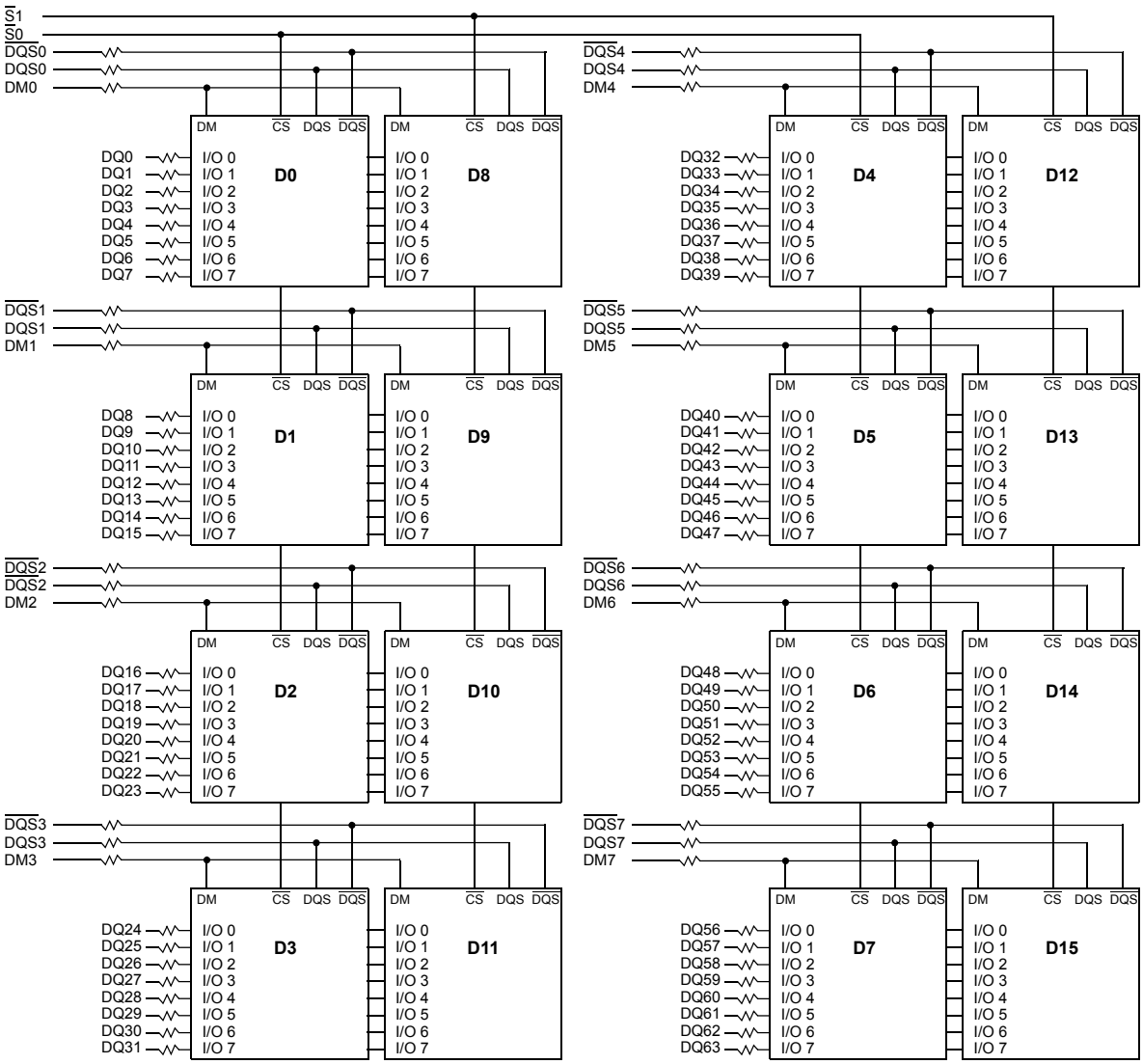
7.0 Input/Output Function Description

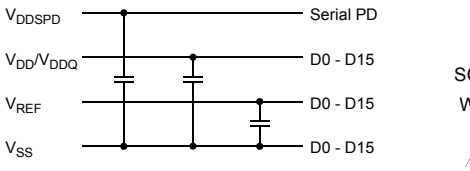
Symbol	Type	Description
CK0-CK2 CK0-CK2	Input	CK and $\overline{CK}$ are differential clock inputs. All the SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of CK. Output (read) data is reference to the crossing of CK and CK (Both directions of crossing)
CKE0-CKE1	Input	Activates the SDRAM CK signal when high and deactivates the CK Signal When low. By deactivating the clocks, CKE low initiates the Powe Down mode, or the Self-Refresh mode
$\overline{S}$0-$\overline{S}$1	Input	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disbled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (ALONG WITH CS) define the command being entered.
ODT0-ODT1	Input	When high, termination resistance is enabled for all DQ, $\overline{DQ}$ and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).
V_{REF}	Supply	Reference voltage for SSTL 18 inputs.
V_{DDQ}	Supply	Power supply for the DDR II SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins.
BA0-BA2	Input	Selects which SDRAM BANK of four is activated.
A0-A14	Input	During a Bank Activate command cycle, Address input defines the row address (RA0-RA14) During a Read or Write command cycle, Address input defines the colum address, In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BA2 defines the bank to be precharged. If AP is low, autoprecharge is disbled. During a precharge command cycle, AP is used in conjunction with BA0-BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BA2. If AP is low, BA0, BA1, BA2 are used to define which bank to precharge.
DQ0-DQ63 CB0-CB7	In/Out	Data and Check Bit Input/Output pins.
DM0-DM8	Input	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD},V_{SS}	Supply	Power and ground for DDR2 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules.
DQS0-DQS8 DQS0-DQS8	In/Out	Data strobe for input and output data. For Rawcards using x16 orginized DRAMs DQ0-7 connect to the LDQS pin of the DRAMs and DQ8-17 connect to the UDQS pin of the DRAM
SA0-SA2	Input	These signals and tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EERPOM address range.
SDA	In/Out	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup on the system board.

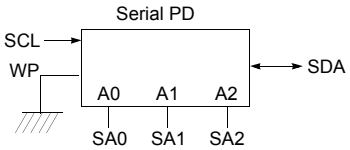
8.0 Functional Block Diagram :

8.1 4GB, 512Mx64 Module - M378T5263AZ(H)3

(Populated as 2 rank of x8 DDR2 SDRAMs)







BA0 - BA2	BA0-BA2 : DDR2 SDRAMs D0 - D15
A0 - A14	A0-A14 : DDR2 SDRAMs D0 - D15
CKE0	CKE : DDR2 SDRAMs D0 - D7
CKE1	CKE : DDR2 SDRAMs D8 - D15
$\overline{RAS}$	$\overline{RAS}$: DDR2 SDRAMs D0 - D15
$\overline{CAS}$	$\overline{CAS}$: DDR2 SDRAMs D0 - D15
$\overline{WE}$	$\overline{WE}$: DDR2 SDRAMs D0 - D15
ODT0	ODT : DDR2 SDRAMs D0 - D7
ODT1	ODT : DDR2 SDRAMs D8 - D15

* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/$\overline{CK0}$	4 DDR2 SDRAMs
*CK1/$\overline{CK1}$	6 DDR2 SDRAMs
*CK2/$\overline{CK2}$	6 DDR2 SDRAMs

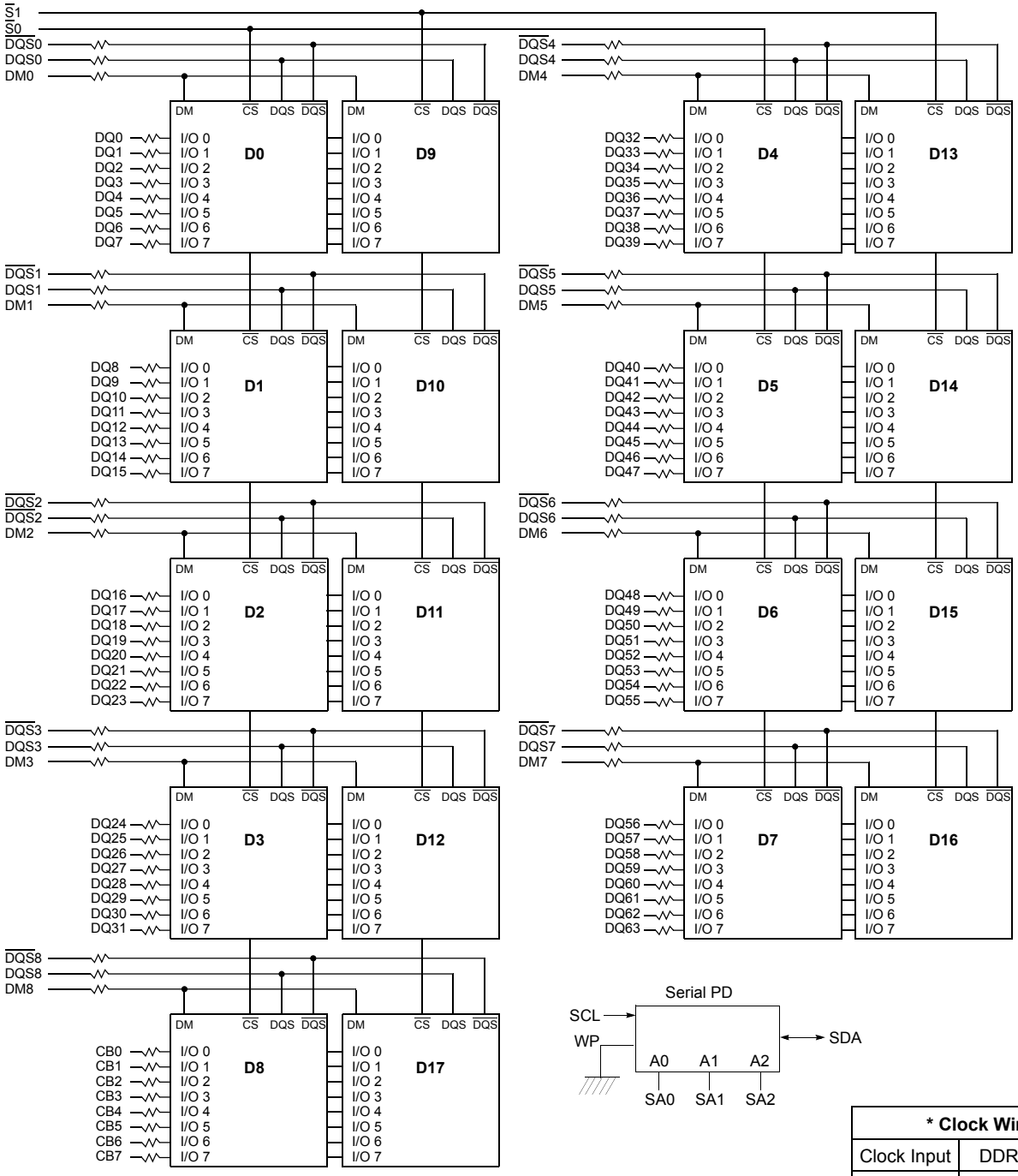
*Wire per Clock Loading Table/Wiring Diagrams

Note :

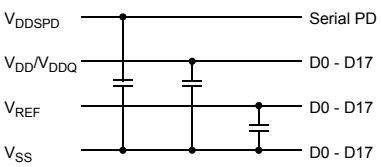
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 7.5 Ohms ± 5%.

8.2 4GB, 512Mx72 ECC Module - M391T5263AZ(H)3

(Populated as 2 rank of x8 DDR2 SDRAMs)



BA0 - BA2 → BA0-BA2 : DDR2 SDRAMs D0 - D17
A0 - A14 → A0-A14 : DDR2 SDRAMs D0 - D17
CKE0 → CKE : DDR2 SDRAMs D0 - D8
CKE1 → CKE : DDR2 SDRAMs D9 - D17
$\overline{RAS}$ → $\overline{RAS}$: DDR2 SDRAMs D0 - D17
$\overline{CAS}$ → $\overline{CAS}$: DDR2 SDRAMs D0 - D17
$\overline{WE}$ → $\overline{WE}$: DDR2 SDRAMs D0 - D17
ODT0 → ODT : DDR2 SDRAMs D0 - D8
ODT1 → ODT : DDR2 SDRAMs D9 - D17



* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/$\overline{CK0}$	6 DDR2 SDRAMs
*CK1/$\overline{CK1}$	6 DDR2 SDRAMs
*CK2/$\overline{CK2}$	6 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

Note :

1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 7.5 Ohms ± 5%.

9.0 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	- 1.0 V ~ 2.3 V	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

10.0 AC & DC Operating Conditions

10.1 Recommended DC Operating Conditions (SSTL - 1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	4
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	4
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1,2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

Note : There is no specific device V_{DD} supply voltage requirement for SSTL-1.8 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.

1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed +/-2% V_{REF}(DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

10.2 Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Operating Temperature	0 to 95	°C	1, 2

Note :
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

10.3 Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(DC)	DC input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
V_{IL}(DC)	DC input logic low	- 0.3	V_{REF} - 0.125	V	

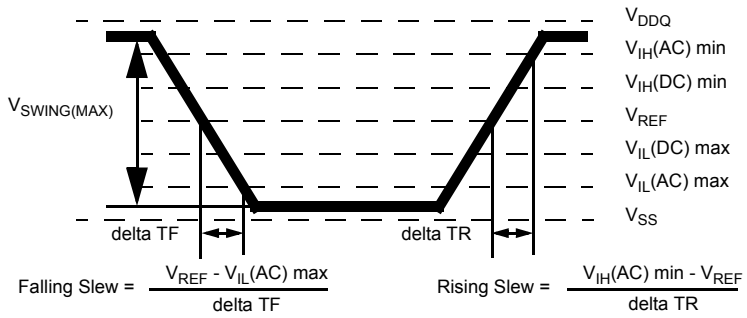
10.4 Input AC Logic Level

Symbol	Parameter	DDR2-533		DDR2-667, DDR2-800		Units	Notes
		Min.	Max.	Min.	Max.		
V_{IH}(AC)	AC input logic high	V_{REF} + 0.250	-	V_{REF} + 0.200		V	
V_{IL}(AC)	AC input logic low	-	V_{REF} - 0.250		V_{REF} - 0.200	V	

10.5 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Notes:
1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}$(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(AC) min for rising edges and the range from V_{REF} to V_{IL}(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V_{IL}(AC) to V_{IH}(AC) on the positive transitions and V_{IH}(AC) to V_{IL}(AC) on the negative transitions.



< AC Input Test Signal Waveform >

11.0 IDD Specification Parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions		Units	Note
IDD0	**Operating one bank active-precharge current;** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD1	**Operating one bank active-read-precharge current;** IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD2P	**Precharge power-down current;** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2Q	**Precharge quiet standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		mA	
IDD2N	**Precharge standby current;** All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD3P	**Active power-down current;** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	mA	
		Slow PDN Exit MRS(12) = 1mA	mA	
IDD3N	**Active standby current;** All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		mA	
IDD5B	**Burst auto refresh current;** tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		mA	
IDD6	**Self refresh current;** CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	mA	
		Low Power	mA	
IDD7	**Operating bank interleave read current;** All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		mA	

12.0 Operating Current Table :

12.1 M378T5263AZ(H)3 : 4GB(256Mx8 *16) Module

(T_A=0°C, V_{DD}= 1.9V)

Symbol	800@CL=5	800@CL6	667@CL=5	533@CL=4	Units	Notes
	CE7	CF7	CE6	CD5		
IDD0	1,240	1,240	1,160	1,080	mA	
IDD1	1,440	1,440	1,320	1,240	mA	
IDD2P	240	240	240	240	mA	
IDD2Q	880	880	800	720	mA	
IDD2N	960	960	880	800	mA	
IDD3P-F	800	800	640	640	mA	
IDD3P-S	288	288	288	288	mA	
IDD3N	1,120	1,120	1,000	920	mA	
IDD4W	1,840	1,840	1,640	1,440	mA	
IDD4R	2,080	2,080	1,800	1,600	mA	
IDD5	2,720	2,720	2,520	2,400	mA	
IDD6	240	240	240	240	mA	
IDD7	3,280	3,280	3,000	2,720	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

12.2 M391T5263AZ(H)3 : 4GB(256Mx8 *18) ECC Module

(T_A=0°C, V_{DD}= 1.9V)

Symbol	800@CL=5	800@CL=6	667@CL=5	533@CL=4	Units	Notes
	CE7	CF7	CE6	CD5		
IDD0	1,395	1,395	1,305	1,215	mA	
IDD1	1,620	1,620	1,485	1,395	mA	
IDD2P	270	270	270	270	mA	
IDD2Q	990	990	900	810	mA	
IDD2N	1,080	1,080	990	900	mA	
IDD3P-F	900	900	720	720	mA	
IDD3P-S	324	324	324	324	mA	
IDD3N	1,260	1,260	1,125	1,035	mA	
IDD4W	2,070	2,070	1,845	1,620	mA	
IDD4R	2,340	2,340	2,025	1,800	mA	
IDD5	3,060	3,060	2,835	2,700	mA	
IDD6	270	270	270	270	mA	
IDD7	3,690	3,690	3,375	3,060	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

13.0 Input/Output Capacitance

(V_{DD}=1.8V, V_{DDQ}=1.8V, T_A=25°C)

Parameter	Symbol	Min	Max	Units
Non-ECC		M378T5263AZ(H)3		
Input capacitance, CK and $\overline{CK}$	CCK0	-	26	pF
	CCK1	-	28	
	CCK2	-	28	
Input capacitance, CKE and $\overline{CS}$	CI_1	-	42	
Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI_2	-	42	
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	-	10	
ECC		M391T5263AZ(H)3		Units
Input capacitance, CK and $\overline{CK}$	CCK0	-	28	pF
	CCK1	-	28	
	CCK2	-	28	
Input capacitance, CKE and $\overline{CS}$	CI_1	-	44	
Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CI_2	-	44	
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	-	10	

Note : DM is internally loaded to match DQ and DQS identically.

14.0 Electrical Characteristics & AC Timing for DDR2-800/667/533

(0 °C ≤ T_{OPER} ≤ 95 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V)

14.1 Refresh Parameters by Device Density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to active/Refresh command time	tRFC		75	105	127.5	195	327.5	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	7.8	7.8	7.8	7.8	µs
		85 °C < T_{CASE} ≤ 95°C	3.9	3.9	3.9	3.9	3.9	µs

14.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

Speed	DDR2-800(E7)		DDR2-800(F7)		DDR2-667(E6)		DDR2-533(D5)		Units
Bin(CL - tRCD - tRP)	5 - 5 - 5		6 - 6- 6		5 - 5 - 5		4 - 4 - 4		
Parameter	min	max	min	max	min	max	min	max	
tCK, CL=3	5	8	-	-	5	8	5	8	ns
tCK, CL=4	3.75	8	3.75	8	3.75	8	3.75	8	ns
tCK, CL=5	2.5	8	3	8	3	8	3.75	8	ns
tCK, CL=6	-	-	2.5	8	-	-	-	-	ns
tRCD	12.5	-	15	-	15	-	15	-	ns
tRP	12.5	-	15	-	15	-	15	-	ns
tRC	57.5	-	60	-	60	-	60	-	ns
tRAS	45	70000	45	70000	45	70000	45	70000	ns

14.3 Timing parameters by speed grade (DDR2-800 and DDR2-667)

(Refer to notes for informations related to this table at the component datasheet)

Parameter	Symbol	DDR2-800		DDR2-667		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-400	400	-450	450	ps	40
DQS output access time from CK/$\overline{CK}$	tDQSCK	-350	350	-400	400	ps	40
Average clock HIGH pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
Average clock LOW pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
CK half pulse period	tHP	Min(tCL(abs), tCH(abs))	x	Min(tCL(abs), tCH(abs))	x	ps	37
Average clock period	tCK(avg)	2500	8000	3000	8000	ps	35,36
DQ and DM input hold time	tDH(base)	125	x	175	x	ps	6,7,8,21,28,31
DQ and DM input setup time	tDS(base)	50	x	100	x	ps	6,7,8,20,28,31
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK(avg)	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK(avg)	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC(max)	x	tAC(max)	ps	18,40
DQS/$\overline{DQS}$ low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC(min)	tAC(max)	tAC(min)	tAC(max)	ps	18,40
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2* tAC(min)	tAC(max)	2* tAC(min)	tAC(max)	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	200	x	240	ps	13
DQ hold skew factor	tQHS	x	300	x	340	ps	38
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	39
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	-0.25	0.25	tCK(avg)	30
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK(avg)	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK(avg)	30
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK(avg)	30
Mode register set command cycle time	tMRD	2	x	2	x	nCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	32
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10
Write preamble	tWPRE	0.35	x	0.35	x	tCK(avg)	
Address and control input hold time	tIH(base)	250	x	275	x	ps	5,7,9,23,29
Address and control input setup time	tIS(base)	175	x	200	x	ps	5,7,9,22,29
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19,41
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19,42
Activate to activate command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4,32
Activate to activate command period for 2KB page size products	tRRD	10	x	10	x	ns	4,32

Parameter	Symbol	DDR2-800		DDR2-667		Units	Notes
		min	max	min	max		
Four Activate Window for 1KB page size products	tFAW	35	x	37.5	x	ns	32
Four Activate Window for 2KB page size products	tFAW	45	x	50	x	ns	32
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2	x	2	x	nCK	
Write recovery time	tWR	15	x	15	x	ns	32
Auto precharge write recovery + precharge time	tDAL	WR + tnRP	x	WR + tnRP	x	nCK	33
Internal write to read command delay	tWTR	7.5	x	7.5	x	ns	24,32
Internal read to precharge command delay	tRTP	7.5	x	7.5	x	ns	3,32
Exit self refresh to a non-read command	tXSNR	tRFC + 10	x	tRFC + 10	x	ns	32
Exit self refresh to a read command	tXSRD	200	x	200	x	nCK	
Exit precharge power down to any command	tXP	2	x	2	x	nCK	
Exit active power down to read command	tXARD	2	x	2	x	nCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	8 - AL	x	7 - AL	x	nCK	1,2
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3	x	3	x	nCK	27
ODT turn-on delay	tAOND	2	2	2	2	nCK	16
ODT turn-on	tAON	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max)+0.7	ns	6,16,40
ODT turn-on (Power-Down mode)	tAONPD	tAC(min)+2	2*tCK(avg) +tAC(max)+1	tAC(min)+2	2*tCK(avg) +tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	nCK	17,45
ODT turn-off	tAOF	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	17,43,45
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5*tCK(avg) +tAC(max)+1	tAC(min)+2	2.5*tCK(avg) +tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3	x	3	x	nCK	
ODT power down exit latency	tAXPD	8	x	8	x	nCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK(avg) +tIH	x	tIS+tCK(avg) +tIH	x	ns	15

14.4 Timing parameters by speed grade (DDR2-533)

(Refer to notes for informations related to this table at the component datasheet)

Parameter	Symbol	DDR2-533		Units	Notes
		min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-500	500	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-450	450	ps	
CK HIGH pulse width	tCH	0.45	0.55	tCK	
CK LOW pulse width	tCL	0.45	0.55	tCK	
CK half pulse period	tHP	Min(tCL, tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	3750	8000	ps	15
DQ and DM input hold time (differential strobe)	tDH(base)	225	x	ps	6,7,8,21,28
DQ and DM input setup time (differential strobe)	tDS(base)	100	x	ps	6,7,8,20,28
DQ and DM input hold time (single-ended strobe)	tDH1(base)	-25	x	ps	6,7,8,26
DQ and DM input setup time (single-ended strobe)	tDS1(base)	-25	x	ps	6,7,8,25
Control & Address input pulse width for each input	tIPW	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC(max)	ps	18
DQS(/$\overline{DQS}$) low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC(min)	tAC(max)	ps	18
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2* tAC(min)	tAC(max)	ps	18
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	300	ps	13
DQ hold skew factor	tQHS	x	400	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	ps	
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	tCK	
DQS input HIGH pulse width	tDQSH	0.35	x	tCK	
DQS input LOW pulse width	tDQSL	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	tCK	
MRS command to ODT update delay	tMOD	0	12	ns	
Write postamble	tWPST	0.4	0.6	tCK	10
Write preamble	tWPRE	0.35	x	tCK	
Address and control input hold time	tIH(base)	375	x	ps	5,7,9,23
Address and control input setup time	tIS(base)	250	x	ps	5,7,9,22
Read preamble	tRPRE	0.9	1.1	tCK	19
Read postamble	tRPST	0.4	0.6	tCK	19
Active to active command period for 1KB page size products	tRRD	7.5	x	ns	4
Active to active command period for 2KB page size products	tRRD	10	x	ns	4

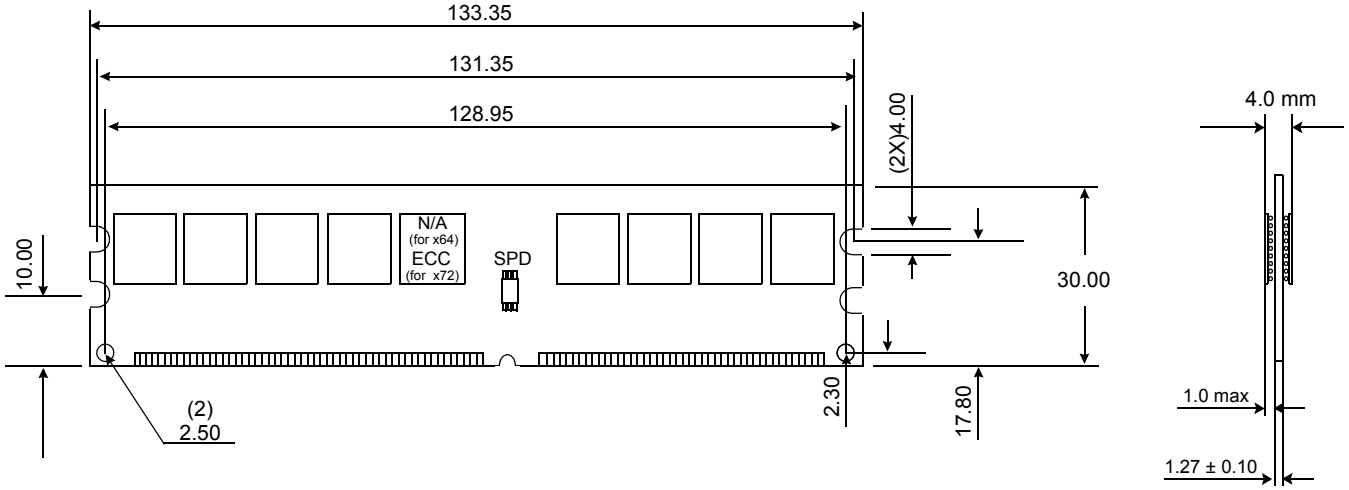
Parameter	Symbol	DDR2-533		Units	Notes
		min	max		
Four Activate Window for 1KB page size products	tFAW	37.5	x	ns	
Four Activate Window for 2KB page size products	tFAW	50	x	ns	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2	x	tCK	
Write recovery time	tWR	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	x	tCK	14
Internal write to read command delay	tWTR	7.5	x	ns	24
Internal read to precharge command delay	tRTP	7.5	x	ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10	x	ns	
Exit self refresh to a read command	tXSRD	200	x	tCK	
Exit precharge power down to any non-read command	tXP	2	x	tCK	
Exit active power down to read command	tXARD	2	x	tCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	6 - AL	x	tCK	1,2
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3	x	tCK	27
ODT turn-on delay	tAOND	2	2	tCK	16
ODT turn-on	tAON	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	tCK	17,44
ODT turn-off	tAOF	tAC(min)	tAC(max) + 0.6	ns	17,44
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3	x	tCK	
ODT power down exit latency	tAXPD	8	x	tCK	
OCD drive mode output delay	tOIT	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH	x	ns	15

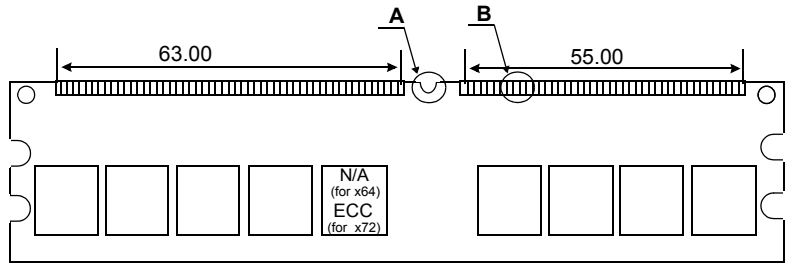
15.0 Physical Dimensions :

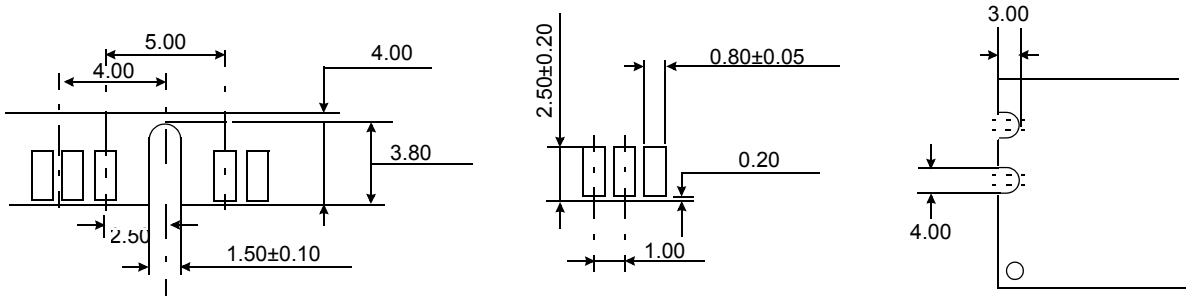
256Mbx8 based 512Mx64(x72) Module(2 Rank)

- M378(91)T5263AZ(H)3

Units : Millimeters







Detail A **Detail B**

The used device is 256M x8 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T2G084QA